REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of May 24, 2006 (hereinafter "Office Action"). In response, Applicants respectfully submit that the cited references do not disclose or suggest, at least, the recitations of the pending independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claim 1 is Patentable

Independent Claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 6,153,455 to Ling et al. (hereinafter "Ling"). Independent Claim 1 is directed to a method of forming a semiconductor device and recites, in part:

> ...
> forming spacers on sidewalls of the gate pattern, the spacers having a bottom width;
> implanting impurity ions using the gate pattern and the spacer as a mask to form a heavily doped impurity diffusion layer in the substrate;
> removing the spacers; and
> forming a conformal etch stop layer on the gate pattern and the substrate after removing the spacers, wherein the etch stop layer is formed to a thickness of at least the bottom width of the spacers.

Thus, according to independent Claim 1, spacers are formed on sidewalls of the gate pattern and are used as a mask to form a heavily doped impurity diffusion layer. The spacers are removed and ***then*** an etch stop layer is formed to have a thickness of at least the bottom width of the spacers.

Ling describes a method of fabricating a transistor in which a combination of the undoped oxide layer 113 and nitride spacers 134* form sidewalls spacers that are used as masks during ion implantation as shown in FIGS. 5 and 6. In sharp contrast to the recitations of independent Claim 1, however, the undoped oxide layer 113, which is alleged to correspond to the etch stop layer, is formed before the nitride spacers 134* are removed. (Ling, FIG. 2--oxide layer 113 formed before spacers 134* are even formed in FIG. 4).

In response to this analysis, the Office Action acknowledges that the oxide layer 113 is formed before the spacers 134* are even formed, much less removed. (Office Action, page 8). The Office Action does, allege, however, that FIG. 1 and col. 4, lines 16-35 and 63-65 of Ling discloses "forming highly doped regions by implanting on the CMOS transistor/gate pattern..., which reads on implanting impurity ions using the gate pattern and the spacer as a mask to form a heavily doped impurity diffusion layer in the substrate and Ling also discloses that the conformal etch stop layer 113 is formed after the spacers (formed on the sidewall of gate structure 120 as seen in fig. 1 of Ling) are removed (figs. 1-2)." (Office Action, pages 8-9).

Applicants respectfully submit that the Office Action appears to misinterpret the teachings of Ling. The spacers shown on the sidewalls of the gates 120 and 122 shown in FIG. 1 of Ling are not removed in FIG. 2 of Ling. Rather, FIG. 1 of Ling illustrates the resulting structure of a CMOS transistor 10 that is formed in accordance with the fabrications methods shown in FIGS. 2 – 10 of Ling. (See Ling, col. 4, lines 18-19 and 46 – 48). Applicants submit, therefore, that the spacers 121* shown in FIGS. 1, and 8 – 10, for example, are not used as a mask for implanting impurity ions to form a heavily doped impurity diffusion layer as recited in independent Claim 1. Instead, Ling teaches that spacers 121* are used to form lightly doped regions 222* and 234* as shown in FIGS. 9 and 10 and described at col. 9, lines 11-42. Moreover, the spacers 121* are not removed before forming the alleged etch stop layer 113, but are instead formed by etching the undoped oxide layer 113 as shown in FIG. 8 and discussed at col. 6, line 64 through col. 7, line 10.

Applicants submit, therefore, that Ling does not disclose, at least, the use of spacers to form a heavily doped impurity diffusion layer, which are then removed before forming a conformal etch stop layer on the gate pattern and substrate as recited in independent Claim 1.

Independent Claim 1 also stands rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,451,704 to Pradeep et al. (hereinafter "Pradeep"). The Office Action alleges that the oxide layer 32 shown in FIG. 4 of Pradeep corresponds to the etch stop layer recited in independent Claim 1. (Office Action, page 4). Applicants respectfully disagree that the oxide layer 32 is an etch stop layer. Instead, the oxide layer 32 is etched to form

second gate spacers 32 as shown in FIG. 5 using the same etching techniques as were used to form the first gate spacers 24 of FIG. 2. (Pradeep, col. 9, lines 17 - 38). Applicants submit, therefore, that the oxide layer 32 cannot correspond to the etch stop layer recited in Claim 1.

In response to this analysis, the Office Action states that the oxide layer 32 qualifies as an etch stop layer because it allegedly protects the layer 21 from being etched from the sidewalls of the gate electrodes 14 and 16 as shown in FIG. 5. (Office Action, page 9). Applicants respectfully disagree with this interpretation of the function of the oxide layer 32. Applicants submit that the oxide layer 32 does not protect the layer 21 from being etched, but rather the etching process is designed so as to etch the layer 32 such that portions remain on the sidewalls of the gate electrodes 14 and 16. Pradeep explains at col. 9, lines 25 – 29 that the spacers 32 shown in FIG. 5 are formed by design. The etching process of layer 32 used to form the spacers 32 on the sidewalls of the gate electrodes 14 and 16 removes all of layer 32 from the device except for the spacers, which are intentionally not etched. Thus, the spacers 32 do not protect the layer 21 from an etchant as the spacers 32 are intentionally not etched by design.

Although Applicants do not agree, assuming for the sake of argument that the oxide layer 32 does qualify as an etch stop layer because the spacers 32 protect the layer 21 from being etched, Applicants respectfully submit that the oxide layer does not qualify as a conformal etch stop layer that is formed on the gate pattern and the substrate as recited in independent Claim 1. That is, while the layer 32 is conformally formed on the gate electrodes 14 and 16 and the substrate 10, it does not function as a conformal etch stop layer because it is readily etched from the top of the electrodes 14 and 16 and the surface of the substrate 10 between the electrodes 14 and 16 as shown in FIG. 5 and described at col. 9, lines 25 – 37 of Pradeep.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 1 is patentable over Ling and Pradeep, either alone or in combination, and that Claims 2 - 11 are patentable at least per the patentability of independent Claim 1.

Independent Claim 12 is Patentable

Independent Claim 12 stands rejected under 35 U.S.C. §102(e) as being anticipated by Pradeep. Independent Claim 12 is directed to a method of forming a semiconductor device and recites, in part:

> ...
> forming spacers on sidewalls of the first and second gate patterns, the sidewall spacers having a bottom width;
> forming a heavily doped impurity diffusion layer in the first active region using the first gate pattern and the spacers on the sidewalls of the first gate pattern as a mask;
> removing the spacers; and
> forming a conformal etch stop layer on the first and second gate patterns and the substrate after removing the spacers,
> wherein the second gate pattern is formed to cross over the device isolation layer and to reach the first active region, and
> wherein the etch stop layer is formed to a thickness of at least the bottom width of the sidewall spacers.

Thus, according to independent Claim 12, spacers are formed on sidewalls of the gate patterns and are used as a mask to form a heavily doped impurity diffusion layer. The spacers are removed and ***then*** an etch stop layer is formed to have a thickness of at least the bottom width of the spacers.

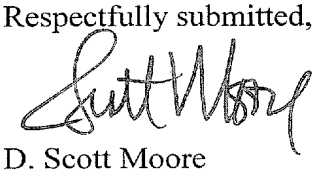
As discussed above with respect to independent Claim 1, the Office Action alleges that the oxide layer 32 shown in FIG. 4 of Pradeep corresponds to the etch stop layer recited in independent Claim 1. (Office Action, page 5). Applicants respectfully submit that the oxide layer 32 is not an etch stop layer nor is the oxide layer 32 a conformal etch stop layer for the reasons discussed above with respect to the rejection of independent Claim 1. Applicants submit, therefore, that the oxide layer 32 cannot correspond to the etch stop layer recited in Claim 12.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 12 is patentable over Pradeep, and that Claims 13 - 21 are patentable at least per the patentability of independent Claim 12.

CONCLUSION

In light of the above remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

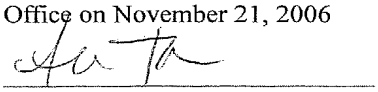


D. Scott Moore
Registration No. 42,011

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 20792

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted electronically to the U.S. Patent and Trademark Office on November 21, 2006



Amelia Tauchen